Abstracts

Modeling and analysis techniques for system-level architectural design of telecom front-ends

G.G.E. Gielen. "Modeling and analysis techniques for system-level architectural design of telecom front-ends." 2002 Transactions on Microwave Theory and Techniques 50.1 (Jan. 2002, Part II [T-MTT] (Special Issue on Silicon-Based RF and Microwave Integrated Circuits)): 360-368.

An overview is presented of the challenges and design issues in the system-level design of mixed analog-digital telecom front-ends. The progress in very large scale integration technology allows the integration of complex systems on a chip, containing both analog and digital parts. In order to boost the design productivity and guarantee the optimality of such systems while meeting the time-to-market constraints, a systematic top-down design approach has to be followed with sufficient time and attention paid to system-level architectural design before proceeding to the detailed block or circuit design. This paper presents high-level system exploration tools that allow the analysis of architectural alternatives for the telecom front-end and to explore system tradeoffs such as finding the optimal analog-digital partitioning. This is illustrated with results from experimental tools. Finally, the crucial underlying technology for such high-level design will be described in detail: analog behavioral modeling, efficient high-level simulation methods, and analog power/area estimation.

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